REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of March 29, 2004 is respectfully requested.

In order to make necessary editorial corrections, the entire specification and abstract have been reviewed and revised, and the changes have been incorporated as shown above. No new matter has been added by the revisions.

In view of the Election of Invention I, filed January 5, 2004, claims 11-14 have been withdrawn from further consideration. Furthermore, elected claims 1-3 and 7-10 have been rejected under 35 USC § 102(b) as being anticipated by the Jin reference (USP 6,350,665) or the Jain reference (U.S. Application 2002/0055250). In addition, elected dependent claims 4-6 have been rejected under 35 USC § 103(a) as being unpatentable over the Jin reference or the Jain reference. However, as indicated above, original claims 1-14 have been cancelled and replaced with new claims 15-34, including new independent claims 15, 27, 29, and 32. It is submitted that all of the new claims read on the elected Invention I. Furthermore, for the reasons discussed below, it is respectfully submitted that new claims 15-34 are clearly patentable over the prior art of record.

New independent claims 15 and 32 are both directed to a contact hole formation method, comprising forming a first group of gate electrodes on a first region of a substrate so that the first group of gate electrodes are *densely arranged*, and forming a second group of gate electrodes on a second region of the substrate so that the second group of gate electrodes are *sparsely arranged*. A first dielectric film is deposited on the first region and the second region of the substrate on which the gate electrodes are formed, and the first dielectric film is planarized. A second dielectric film is deposited on the planarized first dielectric film, and contact holes are formed through the first dielectric film and the second dielectric film. New independent claim 27 is directed to a contact hole formation method similar to the method recited in independent claim 15, except that instead of forming a first group and a second group of *gate electrodes*, independent claim 27 recites that the method comprises forming a first group of *interconnections* on a first region of a substrate so that the first group of interconnections are

densely arranged, and forming a second group of interconnections on a second region of the substrate so that the second group of interconnections are *sparsely arranged*.

The invention recited in new independent claims 15, 27, and 32 provides several advantages. Firstly, a first group of gate electrodes or interconnections are densely arranged on a first region of a substrate, while a second group of gate electrodes or interconnections are sparsely arranged on a second region of the substrate. Thus, a semiconductor device including the substrate and the gate electrodes or interconnections can provide a high degree of integration and flexibility. Furthermore, as explained in paragraph [0043] spanning pages 17-19 of the specification, because the second dielectric film is deposited on a *planarized* first dielectric film, the variation in etching rates for each of the contact holes can be minimized or eliminated. Thus, contact holes formed through the first dielectric film and the second dielectric film can be formed to a uniform depth. As a result, problems such as current leakage or poor electrical connections can be avoided (see, in particular, lines 1-8 on page 19 of the specification in this regard).

The Jin reference is directed to a method of producing contacts in a semiconductor structure, in which a first gate structure 600-0 and a second gate structure 600-1 are formed on a substrate 602. An interlayer dielectric 620 is formed on the substrate 602, and a cap interlayer dielectric 634 is formed on the planarized interlayer dielectric 620. However, as illustrated in Figures 6A through 6T, and described in, for example, column 12, line 35 through column 13, line 5 of the Jin reference, the gate structures arranged on the substrate 602 are all evenly spaced apart. In other words, the Jin reference does not disclose or even suggest a first group of gate electrodes or interconnections on a first region of a substrate so that the first group of interconnections are *densely arranged*, and a second group of interconnections or gate electrodes on a second region of the substrate so that the second group of interconnections are *sparsely arranged*. In fact, the Jin reference does not even suggest the necessity for forming a first group of gate electrodes or interconnections in a densely-arranged manner on a first region, and a second group of interconnections or gate electrodes in a sparsely-arranged manner on a second region. Thus, it is respectfully submitted that the Jin reference does not anticipate or even suggest the invention recited in new independent claims 15, 27, or 32.

The Jain reference is directed to a dielectric structure, including a transistor 102 formed on a semiconductor body 100. A dielectric layer 110 including a doped oxide layer 112 and a stopping layer 114 is formed on the semiconductor body 100, and a trench 106 is formed through the dielectric layer 110. However, the Jain reference does not disclose or even suggest forming a first group of interconnections or gate electrodes on a first region of a substrate in a *densely-arranged* manner, and forming a second group of interconnections or gate electrodes on a second region of the substrate in a *sparsely-arranged* manner. Thus, it is respectfully submitted that the Jain reference does not anticipate or even suggest the invention recited in new independent claims 15, 27, and 32.

As explained above, the Jin reference and the Jain reference do not, either alone or in combination, disclose or suggest a contact hole formation method including the combination of forming a first group of interconnections or gate electrodes on a first region of a substrate and a second group of interconnections or gate electrodes on a second region of the substrate, as well as depositing a first dielectric film on the substrate, planarizing the first dielectric film, and depositing a second dielectric film on the planarized first dielectric film, as recited in new independent claims 15, 27, and 32. Therefore, one of ordinary skill in the art would not be motivated to either modify or combine the Jin reference and the Jain reference so as to obtain the invention recited in new independent claims 15, 27, and 32. Accordingly, it is respectfully submitted that independent claims 15, 27, and 32, and the claims that depend therefrom, are clearly patentable over the prior art or record.

New independent claim 29 is directed to a contact hole formation method that comprises forming a plurality of interconnections on a substrate, in which the interconnections include a first interconnection and second interconnection, and in which the width of the first interconnection is different than the width of the second interconnection. A first dielectric film is deposited on the substrate on which the interconnections are formed, and the first dielectric film is planarized. A second dielectric film is deposited on the planarized first dielectric film, and contact holes are formed through the first dielectric film and the second dielectric film.

As with the invention recited in claims 15, 27, and 32, forming interconnections having different widths on a substrate allows a resulting semiconductor device to provide a high degree of integration and flexibility. Furthermore, depositing the second dielectric film on a planarized

first dielectric film minimizes the variation in etching rates for each of the contact holes. Thus, contact holes formed through the first dielectric film and the second dielectric film can be formed to a uniform depth. As a result, problems such as current leakage or poor electrical connections can be avoided.

As noted above, the Jin reference discloses the formation of a first gate structure 600-0 and a second gate structure 600-1 on a substrate 602. However, as illustrated in Figures 6A-6T, the gate structures have *identical* widths. Thus, the Jin reference does not disclose or even suggest forming a plurality of interconnections on a substrate, including a first interconnection that has a width different than a width of a second interconnection. Thus, it is respectfully submitted that the Jin reference does anticipate or even suggest the invention recited in new independent claim 29.

As also noted above, the Jain reference discloses the formation of a transistor 102 on a semiconductor body 100. However, the Jain reference also does not disclose or suggest the formation of a plurality of interconnections on a substrate, in which a first interconnection has a width different than a width of a second interconnection. Thus, it is respectfully submitted that the Jain reference also does not anticipate or even suggest the invention recited in new independent claim 29.

As explained above, the Jin reference and the Jain reference do not, either alone or in combination, disclose or suggest the formation of a plurality of interconnections on a substrate, in which a first connection has a width different than a width of a second connection, and in which a first dielectric film is deposited on the substrate, the first dielectric film is planarized, and a second dielectric film is deposited on the planarized first dielectric film. Therefore, one of ordinary skill in the art would not be motivated to modify or combine the Jin reference and the Jain reference to obtain the invention recited in new independent claim 29. Accordingly, it is respectfully submitted that new independent claim 29 and the claims that depend therefrom are clearly patentable over the prior art of record.

In addition to the distinctions discussed above with respect to the independent claims, the dependent claims recite additional distinguishing features of the present invention. In particular, new dependent claims 18-20, which correspond to original claims 4-6, respectively, recite the

elimination of a precipitate from the surface of the first dielectric film, or the formation of the second dielectric film before the formation of the precipitate. Thus, any potential reduction in yield during the semiconductor device manufacturing process is eliminated (see, for example, paragraph [0024] of the specification).

In the Office Action, the Examiner asserted that the subject matter recited in original dependent claims 4-6 would have been obvious to one of ordinary skill in the art, although the Examiner did not provide any evidence or teaching to support this position. In this regard, the Federal Circuit has clearly established that a rejection based on hindsight is improper. See, e.g., *In re Dembiczek* 175 F.3d 994,999, 50 USPQ2d 1614,1617 (Fed Cir. 1999) ("our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.") Furthermore, the Federal Circuit has required specific evidence that the combination of reference in an obviousness rejection teach all of the elements of the claimed invention. See, e.g., *In re Kotzab*, 217 F.3d 1365,1371, 55 USPQ2d 1313,1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"). In the present case, however, the Examiner has used mere hindsight in the rejection of original claims 4-6, which correspond to new dependent claims 18-20, and has not provided any evidence or teachings to support his position regarding the lack of precipitate. Furthermore, it is submitted that the prior art references of record do not disclose or even suggest the subject matter recited in new dependent claims 18-20. Therefore, in view of the reasons discussed above, in addition to the reasons discussed above with respect to the independent claims, it is respectfully submitted that the invention recited in dependent claims 18-20 are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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July 29, 2004